IN THE UNITED STATES PATENT & TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **JUAN-ANTONIO CARBELLO**	§	Attorney Docket No.: **AUS920030655US1**
Serial No.: **10/687,257**	§	Examiner: **BURD, KEVIN M.**
Filed: **OCTOBER 16, 2003**	§	Group Art Unit: **2611**
Title: **CHANNEL-BASED TESTING OF COMMUNICATION LINK**	§	Confirmation No.: **9980**

APPEAL BRIEF UNDER 37 C.F.R. 1.192

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Sir:

This Appeal Brief is submitted in support of the Appeal of the Examiner's final rejection the claims of the above-identified application.

REAL PARTY IN INTEREST

The real party in interest in the present Appeal is International Business Machines Corporation, the Assignee of the present application.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, the Appellant's legal representative, or assignee, which directly affect or would be directly affected by or have a bearing on the Board's decision in the pending Appeal.

STATUS OF CLAIMS

Claims 1-20 were originally presented. No claims were canceled or entered during prosecution. Claims 1-20, which comprise all pending claims, stand finally rejected by the Examiner as noted in the Final Office Action dated July 31, 2007. The rejection of each of Claims 1-20 is appealed.

STATUS OF AMENDMENTS

Appellant's Amendment A, filed May 29, 2007, was entered by the Examiner. No amendment to the claims has been proposed or entered subsequent to the final rejection that led to this appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1 recites a communication link for use in a data processing system. As illustrated at Figure 2, reference numeral 150 and as described *inter alia* at page 6, lines 7-14 of the present specification, the communication link includes a receive interface (e.g., receive interface 152) to receive and convert the voltage levels of a test signal carrying a clock signal and a test data signal. As depicted at Figure 2, reference numeral 170 and as described *inter alia* at page 6, lines 7-14 of the present specification, the communication link includes a clock/data recovery (CDR) circuit coupled to the receive interface and enabled to extract the clock signal and the test data signal from the received signal. As illustrated at reference numeral 160 of Figure 2 and as described *inter alia* at page 6, lines 15-26 of the present specification, the communication link includes a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the

communication link. As illustrated in Figure 3, reference numeral 166 and as described *inter alia* at page 8, lines 1-24 of the present specification, the debug unit further includes a test advisor configured to output a recommendation regarding a communication problem, based on the BER and the at least one jitter characteristic.

Dependent Claim 4 recites, in addition to the features of Claim 1, that the recommendation of the test advisor indicates at least one additional test to be performed when the BER exceeds a predetermined threshold and each of the at least one jitter characteristics is acceptable (see, e.g., Figure 4, reference numeral 202 and page 9, lines 25-28 of the present specification).

Dependent Claim 5 recites, in addition to the features of Claims 1 and 4, that the at least one additional test includes the use of a jitter tolerance pattern (see, e.g., Figure 4, reference numeral 202 and page 9, lines 25-28 of the present specification).

Dependent Claim 6 recites, in addition to the features of Claim 1, that the recommendation of the test advisor indicates a modification to a characteristic of the clock-data recovery (CDR) circuit to be made when the BER exceeds a predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold (see, e.g., Figure 4, reference numeral 196 and page 9, lines 17-22 of the present specification).

Dependent Claim 7 recites, in addition to the features of Claims 1 and 6, that the at least one jitter characteristic includes a high frequency jitter of the communication link and the modification to the clock-data recovery (CDR) circuit comprises a modification to a rate of sampling the transmitted signal by the clock-data recovery (CDR) circuit when the high frequency jitter of the communication link exceeds the specified threshold (see, e.g., Figure 4, reference numeral 196 and page 9, lines 17-22 of the present specification).

Dependent Claim 8 recites, in addition to the features of Claims 1 and 6, that the at least one jitter characteristic includes a frequency offset of the communication link and the modification to the clock-data recovery (CDR) circuit comprises modification to a bandwidth of

the clock-data recovery (CDR) circuit when the frequency offset of the communication link exceeds the specified threshold (see, e.g., Figure 4, reference numeral 198 and page 9, lines 22-25 of the present specification).

Independent Claim 11 recites a data processing system including a first device connected to a communication channel (see, e.g., Figure 2, reference numeral 106 and page 4, line 25 through page 5, line 7 of the present specification). The first device includes a communication link having a pattern generator (see, e.g., Figure 2, reference numeral 134 and page 6, lines 1-6 of the present specification) and a transmit interface to convert a test pattern generated by the pattern generator to a test data signal for transmission via the communication channel (see, e.g., Figure 2, reference numeral 132 and page 5, lines 22-31 of the present specification). The data processing system also includes a second device, connected to the communication channel (see, e.g., Figure 1, reference numeral 122 and page 4, lines 26-29 of the present specification). The second device contains a communication link receiver including a receive interface to receive and convert the voltage levels of the test data signal that carries a clock signal and a test data signal (see, e.g., Figure 2, reference numeral 152 and page 6, lines 7-14 of the present specification). The communication link receiver also includes a clock/data recovery (CDR) circuit coupled to the receive interface and enabled to extract the clock signal and the test data signal from the received signal (see, e.g., Figure 2, reference numeral 170 and page 6, lines 7-14 of the present specification). The communication link receiver also includes a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the communication link (see, e.g., Figure 2, reference numeral 160 and page 6, lines 15-26 of the present specification). The debug unit further includes a test advisor configured to recommend, based on the BER and the at least one jitter characteristic, corrective action responsive to the BER exceeding a predetermined threshold (see, e.g., Figure 3, reference numeral 166 and page 8, lines 1-24 of the present specification).

Dependent Claim 12 recites, in addition to the features of Claim 11, that the corrective action recommended by the test advisor includes performing at least one additional test when the BER exceeds the predetermined threshold and each of the at least one jitter characteristics is

acceptable (see, e.g., Figure 4, reference numeral 202 and page 9, lines 25-28 of the present specification).

Dependent Claim 13 recites, in addition to the features of Claim 11, that the corrective action recommended by the test advisor includes modifying a characteristic of the clock-data recovery (CDR) circuit when the BER exceeds the predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold (see, e.g., Figure 4, reference numeral 196 and page 9, lines 17-22 of the present specification).

Dependent Claim 14 recites, in addition to the features of Claims 11 and 13, that the corrective action includes modifying a rate of sampling the transmitted signal by the clock-data recovery (CDR) circuit when the at least one jitter statistic that exceeds the specified threshold is a statistic indicative of high frequency jitter of the communication link (see, e.g., Figure 4, reference numeral 196 and page 9, lines 17-22 of the present specification).

Dependent Claim 15 recites, in addition to the features of Claims 11 and 13, that the corrective action includes modifying a bandwidth of the clock-data recovery (CDR) circuit when the at least one jitter statistic that exceeds the specified threshold is a statistic indicative of a frequency offset of the communication link (see, e.g., Figure 4, reference numeral 198 and page 9, lines 22-25 of the present specification).

Independent Claim 18 recites an integrated circuit including a transceiver including a receive interface suitable for connecting the integrated circuit to a serial communication channel (see, e.g., Figure 2, reference numeral 152 and page 6, lines 7-14 of the present specification). The integrated circuit also includes a clock/data recovery (CDR) circuit connected to the receive interface and configured to extract a clock signal and a test data signal from a signal received via the communication channel (see, e.g., Figure 2, reference numeral 170 and page 6, lines 7-14 of the present specification). The integrated circuit further includes a debug unit (see, e.g., Figure 2, reference numeral 150 and page 6, lines 15-26 of the present specification). In the manner permitted by 35 U.S.C. § 112, paragraph 6, Claim 18 recites that the debug unit includes means for determining a bit error rate (BER) of the test data signal (see, e.g., Figure 3, reference

numeral 164 and page 7, lines 27-31 of the present specification), means for determining at least one jitter characteristic of the communication link (see, e.g., Figure 3, reference numeral 162 and page 7, lines 9-26 of the present specification), and means for using the BER and the at least one jitter characteristic to generate an action recommendation if the BER exceeds a specified threshold (see, e.g., Figure 3, reference numeral 166 and page 8, lines 1-24 of the present specification).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The ground of rejection to be reviewed on appeal is the final rejection of Claims 1-9, 11-16 and 18-19 under 35 U.S.C. § 102(e) as unpatentable over U.S. Patent Publication No. 2003/0227989 to *Rhee et al.* (*Rhee*).

The outcome of the review of the foregoing rejection under 35 U.S.C. § 102 will be dispositive of the rejection of Claims 10, 17 and 20 under 35 U.S.C. § 103 as unpatentable over *Rhee* in view of U.S. Patent No. 6,856,206 to *Perrott*.

ARGUMENT

I. The rejection under 35 U.S.C. § 102 in view of *Rhee* should be reversed because *Rhee* does not identically disclose each feature of exemplary Claim 1

In paragraph 4 of the Final Office Action dated July 31, 2007, Claims 1-9, 11-16 and 18-19 are rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent Pub. No. 2003/0227989 to *Rhee et al.* (*Rhee*). That rejection is not well founded and should be reversed because the cited reference does not identically disclose each feature of the present claims.

A. *Rhee* does not disclose the "debug unit" recited in exemplary Claim 1

Exemplary Claim 1 is not rendered unpatentable by *Rhee* because that reference does not identically disclose the debug unit recited in Claim 1 as follows:

> a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the communication link.

In paragraph 4 of the Final Office Action, Figure 2 of *Rhee* and paragraph [0034], which describes *Rhee's* Figure 3, are relied upon as teaching, "The delay locked loop 20 determines if the BER is optimized or not (paragraph 0034) and provides short term jitter tracking (figure 2). The components of the DLL output signals based on these determinations."

Appellant respectfully traverses the Examiner's position because *Rhee's* delay locked loop (DLL) circuit 20 does not identically disclose the "debug unit" recited in exemplary Claim 1 as required to support a rejection under 35 U.S.C. § 102. *Rhee's* delay locked loop (DLL) circuit 20, while perhaps tracking short-term jitter (see, e.g., *Rhee*, paragraph [0032]), does not "determine a bit error rate (BER)" or "determine at least one jitter characteristic" as claimed. At most, the phase detector (PD) within *Rhee's* delay locked loop (DLL) circuit 20 "compares the timing difference between the data transition in the data stream and clock edge ... [and] generates an error voltage" (*Rhee*, paragraph [0005]). No determination of the BER or a jitter characteristic is made.

Because *Rhee* does not disclose the "debug unit" recited in exemplary Claim 1, the rejection of Claim 1 under 35 U.S.C. § 102 should be reversed. In addition, the foregoing remarks overcome the rejections of independent Claims 11 and 18, which similarly recite "a debug unit." The foregoing remarks also overcome the rejection of dependent Claims 2-10, 12-17 and 19-20, which depend from Claims 1, 11 and 18, respectively, and accordingly include the features of their respective underlying independent claims.

B. *Rhee* does not disclosed the "test advisor" recited in exemplary Claim 1

Exemplary Claim 1 is also not rendered unpatentable by *Rhee* because that reference does not identically disclose the test advisor recited in Claim 1 as follows:

> ... the debug unit further includes a test advisor configured to output a recommendation regarding a communication problem, based on the BER and the at least one jitter characteristic.

In paragraph 3 of the Final Office Action the Examiner cites the phase detector (PD) and charge pump (CP) within the delay locked loop (DLL) circuit 20 depicted in *Rhee's* Figure 2 as teaching the claimed "test advisor," stating, "The phase detector and charge pump comprise the test advisor included in the debug unit."

Appellant respectfully traverses the Examiner's position because *Rhee's* delay locked loop (DLL) circuit 20 does not identically disclose the "test advisor" recited in exemplary Claim 1 as required to support a rejection under 35 U.S.C. § 102. Specifically, *Rhee* does not identically disclose that the phase detector (PD) and charge pump (CP) individually or in combination "output a recommendation regarding a communication problem, based on the BER and the at least one jitter characteristic," as recited in exemplary Claim 1. As noted above, the phase detector (PD) within *Rhee's* delay locked loop (DLL) circuit 20 "compares the timing difference between the data transition in the data stream and clock edge ... [and] generates an error voltage" (*Rhee*, paragraph [0005]). In paragraph 3 of the Final Office Action, the Examiner asserts that in response to the error voltage, "The charge pump will output a control signal to adjust the data signal to correct the phase difference." As should be apparent, *Rhee's* phase detector (PD) and charge pump (CP) thus output a signal based solely upon a phase difference, not based on the BER and jitter characteristic determined by the debug unit as claimed.

Because *Rhee* does not teach or suggest "a test advisor configured to output a recommendation regarding a communication problem, based on the BER and the at least one jitter characteristic", Appellant respectfully submits that the rejection of Claim 1 under 35 U.S.C. § 102 should be reversed. In addition, the foregoing remarks overcome the rejections of independent Claims 11 and 18, which respectively recite "a test advisor configured to recommend ... corrective action responsive to the BER exceeding a predetermined threshold" and "means for using the BER and the at least one jitter characteristic to generate an action recommendation if the BER exceeds a specified threshold." The foregoing remarks also overcome the rejection of dependent Claims 2-10, 12-17 and 19-20, which depend from Claims 1, 11 and 18, respectively, and accordingly include the features of their respective underlying independent claims.

II. Rejection of exemplary dependent Claim 4 in view of *Rhee* should be reversed because *Rhee* does not disclose each feature recited in exemplary Claim 4

The rejection of exemplary dependent Claim 4 under 35 U.S.C. § 102 in view of *Rhee* should also be reversed because *Rhee* does not teach or suggest:

> ... the recommendation of the test advisor indicates at least one additional test to be performed when the BER exceeds a predetermined threshold and each of the at least one jitter characteristics is acceptable.

At page 4 of the present Office Action, the Examiner asserts without citation to *Rhee* that "[w]hen the BER is not optimized, an additional correction will be made to correct for the error." This assertion does not provide evidence that *Rhee* identically discloses that "the test advisor indicates at least one additional test to be performed," as recited in Claim 4. Consequently, the rejections of exemplary Claim 4 and similar Claim 12 should be reversed.

III. Rejection of dependent Claim 5 in view of *Rhee* should be reversed because *Rhee* does not disclose each feature recited in Claim 5

The rejection of dependent Claim 5 under 35 U.S.C. § 102 in view of *Rhee* should also be reversed because *Rhee* does not teach or suggest "the at least one additional test includes the use of a jitter tolerance pattern," as recited in Claim 5.

With reference to Claim 5, the Examiner notes at page 4 of the Final Office Action, "Rhee further discloses the present invention controls the clock-and-recovery performance metrics in terms of jitter tolerance in the present invention (paragraph 0034)." Even if accurate, such disclosure by *Rhee* does not identically disclose the use of a jitter tolerance pattern as an additional test as recited in Claim 5. Consequently, the rejection of Claim 5 should be reversed.

IV. Rejection of exemplary dependent Claim 6 in view of *Rhee* should be reversed because *Rhee* does not disclose each feature recited in exemplary Claim 6

The rejection of exemplary dependent Claim 6 under 35 U.S.C. § 102 in view of *Rhee* should also be reversed because *Rhee* does not teach or suggest:

... the recommendation of the test advisor indicates a modification to a characteristic of the CDR circuit to be made when the BER exceeds a predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold.

With reference to Claim 6, the Examiner asserts without citation to *Rhee* that "[w]hen the BER is not optimized, an additional correction will be made to correct for the error" (Final Office Action, page 4). The Examiner's assertion does not provide evidence that *Rhee* identically discloses "the test advisor indicates a modification to a characteristic of the clock-data recovery (CDR) circuit to be made when the BER exceeds a predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold," as recited in Claim 6. Consequently, the rejections of exemplary Claim 6 and similar Claim 13 should be reversed.

V. Rejection of exemplary dependent Claim 7 in view of *Rhee* should be reversed because *Rhee* does not disclose each feature recited in exemplary Claim 7

The rejection of exemplary dependent Claim 7 under 35 U.S.C. § 102 in view of *Rhee* should also be reversed because *Rhee* does not teach or suggest:

said at least one jitter characteristic includes a high frequency jitter of the communication link; and

said modification to the CDR circuit comprises a modification to a rate of sampling the transmitted signal by the CDR circuit when the high frequency jitter of the communication link exceeds the specified threshold.

With reference to Claim 7, the Examiner asserts without citation to *Rhee* that "[w]hen the BER is not optimized, an additional correction will be made to correct for the error" (Final Office Action, page 4). The Examiner's assertion does not provide evidence that *Rhee* identically discloses that the claimed test advisor indicates "a modification to a rate of sampling the transmitted signal by the [clock-data recovery (CDR)] circuit when the high frequency jitter of the communication link exceeds the specified threshold," as recited in Claim 7. Consequently, the rejections of exemplary Claim 7 and similar Claim 14 should be reversed.

VI. Rejection of exemplary dependent Claim 8 in view of *Rhee* should be reversed because *Rhee* does not disclose each feature recited in exemplary Claim 8

The rejection of exemplary dependent Claim 8 under 35 U.S.C. § 102 in view of *Rhee* should also be reversed because *Rhee* does not teach or suggest:

> said at least one jitter characteristic includes a frequency offset of the communication link; and
>
> said modification to the CDR circuit comprises modification to a bandwidth of the CDR circuit when the frequency offset of the communication link exceeds the specified threshold.

With reference to Claim 8, the Examiner asserts without citation to *Rhee* that "[w]hen the BER is not optimized, an additional correction will be made to correct for the error" (Final Office Action, page 4). The Examiner's assertion does not provide evidence that *Rhee* identically discloses that the claimed test advisor indicates a "modification to a bandwidth of the [clock-data recovery (CDR)] circuit when the frequency offset of the communication link exceeds the specified threshold," as recited in Claim 8. Consequently, the rejections of exemplary Claim 8 and similar Claim 15 should be reversed.

VII. Claim rejections under 35 U.S.C. § 103

In paragraph 5 of the present Office Action, Claims 10, 17 and 30 are rejected under 35 U.S.C. § 103(a) as unpatentable by *Rhee* in view of U.S. Patent No. 6,856,206 to *Perrott* (*Perrott*). That rejection should be reversed for the reasons set forth above with respect to the rejection under 35 U.S.C. § 102.

VIII. Conclusion

The foregoing arguments demonstrate that *Rhee*, whether considered individually or in combination with *Perrott*, does not render unpatentable any of the pending claims. Appellant therefore respectfully requests the Board to reverse the rejection of each pending claim.

Appellant has submitted herewith the fee for filing of a Brief in Support of Appeal. No additional fee is believed to be required. If, however, any additional fees are required, please charge those fees to IBM Corporation Deposit Account No. **09-0447**.

Respectfully submitted,

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CLAIMS APPENDIX

1. A communication link for use in a data processing system, comprising:

a receive interface to receive and convert the voltage levels of a test signal transmitted over a communication channel, where the test signal carries a clock signal and a test data signal;

a clock/data recovery (CDR) circuit coupled to the receive interface and enabled to extract the clock signal and the test data signal from the received signal; and

a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the communication link, wherein the debug unit further includes a test advisor configured to output a recommendation regarding a communication problem, based on the BER and the at least one jitter characteristic.

2. The communication link of claim 1, further comprising a transmitter including a transmit interface connected to the communication channel and a pattern generator, wherein the transmit interface is connectable to the pattern generator.

3. The communication link of claim 1, wherein the receive interface is configured to convert non-return to zero (NRZ) formatted serial data to parallel CMOS data.

4. The communication link of claim 1, wherein the recommendation of the test advisor indicates at least one additional test to be performed when the BER exceeds a predetermined threshold and each of the at least one jitter characteristics is acceptable.

5. The communication link of claim 4, wherein the at least one additional test includes the use of a jitter tolerance pattern.

6. The communication link of claim 1, wherein the recommendation of the test advisor indicates a modification to a characteristic of the CDR circuit to be made when the BER exceeds a predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold.

7. The communication link of claim 6, wherein:

said at least one jitter characteristic includes a high frequency jitter of the communication link; and

said modification to the CDR circuit comprises a modification to a rate of sampling the transmitted signal by the CDR circuit when the high frequency jitter of the communication link exceeds the specified threshold.

8. The communication link of claim 6, wherein:

said at least one jitter characteristic includes a frequency offset of the communication link; and

said modification to the CDR circuit comprises modification to a bandwidth of the CDR circuit when the frequency offset of the communication link exceeds the specified threshold.

9. The communication link of claim 1, wherein the CDR circuit includes an edge detector and a phase rotator control unit that is coupled to the debug unit, wherein the phase rotator control unit provides to the debug unit a signal indicative of a frequency offset of the communication link.

10. The communication link of claim 1, wherein the test advisor comprises a look up table (LUT) containing a plurality of entries, each entry having an associated BER value, at least one jitter characteristic value, and one of a plurality of recommendations.

11. A data processing system, comprising:

a first device connected to a communication channel, the first device including a communication link having a pattern generator and a transmit interface to convert a test pattern generated by the pattern generator to a test data signal for transmission via the communication channel;

a second device connected to the communication channel, the second device including a communication link receiver, comprising:

a receive interface to receive and convert the voltage levels of the test data signal transmitted over a communication channel, where the test data signal carries a clock signal and a test data signal;

a clock/data recovery (CDR) circuit coupled to the receive interface and enabled to extract the clock signal and the test data signal from the received signal; and

a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the communication link, wherein the debug unit further includes a test advisor configured to recommend, based on the BER and the at least one jitter characteristic, corrective action responsive to the BER exceeding a predetermined threshold.

12. The system of claim 11, wherein the corrective action recommended by the test advisor includes performing at least one additional test when the BER exceeds the predetermined threshold and each of the at least one jitter characteristics is acceptable.

13. The system of claim 11, wherein the corrective action recommended by the test advisor includes modifying a characteristic of the CDR circuit when the BER exceeds the predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold.

14. The system of claim 13, wherein said corrective action includes modifying a rate of sampling the transmitted signal by the CDR circuit when the at least one jitter statistic that exceeds the specified threshold is a statistic indicative of high frequency jitter of the communication link.

15. The system of claim 13, wherein said correction action includes modifying a bandwidth of the CDR circuit when the at least one jitter statistic that exceeds the specified threshold is a statistic indicative of a frequency offset of the communication link.

16. The system of claim 11, wherein the CDR circuit includes an edge detector and a phase rotator control unit that are each coupled to the debug unit, wherein the edge detector provides to the debug unit a signal indicative of high frequency jitter of the communication link and the

phase rotator control unit provides to the debug unit a signal indicative of a frequency offset of the communication link.

17. The system of claim 11, wherein the test advisor comprises a look up table (LUT) containing a plurality of entries, each entry having an associated BER value, at least one jitter characteristic value, and one of a plurality of recommendations.

18. An integrated circuit, comprising:

a transceiver including a receive interface suitable for connecting the integrated circuit to a serial communication channel;

a clock/data recovery (CDR) circuit connected to the receive interface and configured to extract a clock signal and a test data signal from a signal received via the communication channel;

a debug unit including:

means for determining a bit error rate (BER) of the test data signal;

means for determining at least one jitter characteristic of the communication link; and

means for using the BER and the at least one jitter characteristic to generate an action recommendation if the BER exceeds a specified threshold.

19. The integrated circuit of claim 18, wherein the debug unit includes means for determining high frequency jitter magnitude and frequency offset of the communication link.

20. The integrated circuit of claim 19, wherein the means for generating an action recommendation includes means for accessing a look up table (LUT) to retrieve the action recommendation based on the BER, the high frequency jitter margin and the frequency offset.

EVIDENCE APPENDIX

none

RELATED PROCEEDINGS APPENDIX

none